In Situ Evaluation Method for On-Chip Inductors Using Oscillator Response

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Abstract—It is difficult to obtain the characteristics of on-chip inductors on site since conventional evaluation requires dedicated test devices. In this paper, in-situ evaluation of both inductance and resistance of on-chip inductors without dedicated test devices is proposed, where on-chip inductors are evaluated on the basis of the threshold current for oscillation and oscillation frequency without being affected by lead wires. The proposed method was verified by measurement, and it is found that the error against the evaluation result using a network analyzer is less than 3%.

I. INTRODUCTION

It is indispensable to adopt devices with the necessary characteristics to design a circuit since circuit performance varies depending on the characteristics of elementary devices. Therefore, it is important to evaluate the characteristics of the device precisely, even though a technique for device postprocessing has been reported [1]. The device evaluation is based on the measurement, for which dedicated test devices are necessary. Here, test element group (TEG) evaluation is generally used to obtain the device characteristics. Fig. 1 shows an example of a TEG for on-chip inductors, where all devices under test (DUTs) are connected to their measurement pads. Here, the characteristics of an on-chip device are not determined only by the device structure, but are also influenced by the surrounding of the device. Consequently, although the characteristics in the TEG and those in the circuit are expected to be the same, both are not necessarily the same in a different environment.

To suppress the process variation, on the other hand, a metal density rule is introduced in many processes [2,3]. To satisfy the rule, pattern density is made uniform by allocating dummy patterns, onto the area where the pattern does not exist around the device. This dummy pattern makes the neighborhood environment different in the inductors composing the TEG and those existing in the circuit. This difference causes characteristic variation because electromagnetic field variation is induced. Additionally, since the component devices of the circuit exist in the neighborhood of the on-chip inductor, the dummy pattern is differently allocated according to the metal density in the neighborhood. Due to the different environment in many cases, the characteristics of the inductor in the circuit are not evaluated precisely enough with the TEG. In particular, because the change of the self-resonant frequency of the inductor causes the variation of the tuning range of the VCO, it is necessary to evaluate the inductor in the same environment as the VCO.

Even though a special TEG, which has the same surrounding as used in the circuit, may be designed to obtain sufficiently precise characteristics of the on-chip inductor, a deembedding pattern matched to the wiring for each TEG is required to remove unwanted parasitic components [4, 5] when a network analyzer is utilized for the evaluation. In this case, different inductors generally require their own deembedding patterns, which consume chip area [6]. Although the same deembedding pattern may be used for the fixed positions of an inductor and a measurement pad, the freedom of arrangement is lost.

To overcome this issue, in-situ evaluation of both inductance and resistance of on-chip inductors for the VCO without dedicated test devices is proposed in this paper. In the following sections, the evaluation method of on-chip inductors is described on the basis of the threshold current for oscillation and oscillation frequency without being affected by the parasitic components in lead wires.

II INDUCTOR EVALUATION BASED ON VCO

A. Inductance of the On-Chip Inductor

To realize in-situ evaluation, a symmetric VCO using an LC tank is utilized, the schematic of which is shown in Fig. 2 [7, 8]. A buffer is connected at the output node of the VCO so that the lead wires do not influence the VCO. In an oscillation mode, the conductance of the LC tank is counterbalanced by a negative conductance produced by cross-coupled MOSFETs. The inductance of the on-chip inductor is obtained by the oscillation frequency \( f_0 \) of the VCO and the total capacitance \( C \) as

\[
L = \frac{1}{(2\pi f_0)^2 C}.
\]

Here, \( f_0 \) is obtained using a spectrum analyzer and \( C \) is
calculated by the method described in the following section.

B. Total Capacitance

Since the oscillation frequency is determined by the inductance of an on-chip inductor and the capacitance at both ends of the on-chip inductor, it is necessary to evaluate the \( C \) between the two terminals. As shown in Fig. 3, the \( C \) is determined not only by the varactor, but also by the parasitic capacitances of all devices that compose the VCO. To evaluate the \( C \), Fig. 4 shows the deembedding circuit, in which only an on-chip inductor is removed from the VCO. The capacitance of the deembedding circuit is equal to the capacitance of the VCO without including the inductor. It is noted that the deembedding circuit is unchanged for different on-chip inductors whenever the MOSFETs for the negative resistance with same geometries are used. The equivalent circuit of the deembedding circuit, shown in Fig. 5, is evaluated using the network analyzer. In this measurement, to avoid an unwanted oscillation caused by the negative resistance in the VCO, the cross-coupled wirings are changed in order that the negative resistance becomes a normal (positive) resistance. Finally, the inductance is obtained by (1) [10].

C. Resistance of the On-Chip Inductor

The VCO is considered as a loop of two-stage common-source amplifiers. Assumed that inductor resistance is \( R \) and that the varactor loss is negligible compared with the inductor loss, an open loop gain \( A \) is obtained from

\[
A = (R \cdot g_m)^2, \tag{2}
\]

where \( g_m \) is transconductance of the MOSFET. When assuming that the negative resistance of the crossing coupling is \(-r\),

\[
r = \frac{1}{g_m}. \tag{3}
\]

Since the bias current flowing to the VCO changes \( g_m \), a negative resistance can be adjusted. From (2) and (3), open loop gain is obtained as

\[
A = \left(\frac{R}{r}\right)^2. \tag{4}
\]

Oscillation starts when negative resistances cancel the inductor resistance \( R \), as shown in Fig. 3. Here, \( |R| = |r| \) holds according to Balghauzen’s oscillation condition when steady oscillation is just generated. Therefore, the inductor resistance \( R \) is obtained when \( r \) is increased at which \( R \) cannot be cancelled, where the oscillation stops. This critical point is named a threshold current for oscillation, where \( |R| = |r| \). The oscillation amplitude of the VCO is changed by the change in negative resistance. Although \(-r\) is negative in the actual VCO, its value appears as positive resistance in the same deembedding circuit used for evaluating the total capacitance \( C \). Since the \( r \) is used for evaluating the \( g_m \) and should not include the capacitor loss, a dc analysis is applied for the deembedding circuit although the \( C \) is evaluated by a network analyzer. Finally, the \( r \), at the oscillation threshold, gives the inductor resistance \( R \).

Here, Fig. 6 shows the output amplitude as function of bias current with several different external impedances. The amplitude is reduced with decreasing bias current, and becomes zero at the same bias current independently of the external impedance. As a result, the absolute value of amplitude is unnecessary for evaluation, although one only has to observe the presence of the oscillation from the spectrum and to find the threshold current for oscillation circuit with the spectrum analyzer. Therefore, the loss caused by lead wires need not be corrected.
III MEASUREMENT RESULTS

For verification of the proposed method, on-chip inductors were fabricated with 0.18µm CMOS and measured based on a network analyzer and a VCO. Frequency responses were measured by changing the voltage of the varactor of the VCO. The measurement results are shown in Figs. 7 and 8. The solid line shows the measurements obtained by the conventional method, and the markers show the measurements obtained by the proposed method. Both results agree with each other. According to the evaluation, maximum relative discrepancies of inductance and resistance are both within 3%.

The measurements obtained by proposed method are not influenced by lead wires from the VCO output to the measurement pad. Since the VCO need not be placed in the pad neighborhood, the VCO can be freely placed anywhere. Moreover, selecting switches can be added to separate multiple VCOs electrically since the insertion loss by the switch does not affect the evaluation results. Therefore, several VCOs can be evaluated with shared pads to constitute a matrix connection as shown in Fig. 9. In this case, a VCO can be allocated regardless of the distance from the pad.

A. Area reduction of inductors under test using VCO matrix

Because the pad for the measurement is shared in the VCO matrix, the number of pads can be reduced compared with that for the TEG. Fig. 10 shows a chip micrograph of the VCO matrix. When the area of an inductor is 0.01mm², the number of inductors that can be allocated for the given area is shown in Fig. 11. The area of a pad is 0.01 mm². When four or more inductors are used, the matrix can allocate more inductors than the TEG for the same area. In the conventional method, 7.72 inductors/ mm² can be allocated. On the other hand, in the proposed method, 36.2/ mm² can be allocated. The area can be reduced by 78.7% using the matrix. Because the smaller the size of the inductor connected to the pad, the higher the effect, it is advantageous to measure a minute inductor.

B. Influence of pattern allocated in surrounding

The influence of dishing can be examined by allocating an arbitrary pattern in the inductor surroundings of the VCO. The dummy pattern algorithm used to reduce the variation induced by copper chemical mechanical polishing (Cu-CMP) cannot be optimized now. Only the dummy pattern based on pattern density is widely used. This problem can be experimentally
resolved by obtaining the verification data of a lot of patterns. An arbitrary dummy pattern can be allocated in the surroundings of the DUT in the proposed method.

V CONCLUSION
The characteristics of an inductor actually used in a VCO were evaluated by observing the VCO oscillation. The proposed method, we achieved in-situ evaluation of an on-chip inductor without using a special test device. The error margin rate is within 3%. When four inductors or more are used, the area can be reduced by 78.7% using a matrix.

ACKNOWLEDGMENTS
This work is supported by Semiconductor Technology Academic Research Center (STARC). The chip fabrication was facilitated by the chip fabrication program of VLSI Design and Education Center (VDEC), University of Tokyo, in collaboration with Hitachi, Ltd.

REFERENCES